AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

doping a first region of a semiconductor substrate;

incising the substrate to provide an array of edges having substantially vertical edge surfaces, pairs of the vertical edge surfaces facing one another;

doping a second region ~~regions~~ between each pair ~~the pairs~~ of vertical edge surfaces;

disposing respective ONO structures each providing an electronic memory function ~~on at least some respective ones~~ only on the pairs of the vertical edge surfaces, each ONO structure ~~having a gate insulator formed on an edge surface and~~ extending to the [[a]] doped second region, and a control gate formed on the gate insulator, wherein a first oxide layer of each ONO structure comprises a thicker portion only adjacent to the first region; and

establishing electrical contacts to the first and second regions.

2. (canceled)

3. (currently amended) The method of claim 1, wherein disposing comprises:

~~forming ONO structures on at least some respective ones of the edge surfaces as the gate insulators; and~~

creating respective control gates on the ONO structures, wherein forming ONO structures comprises:

growing a first silicon dioxide from silicon comprising the vertical edge surfaces and second regions of the substrate, wherein the first silicon dioxide is thicker only adjacent to the first region in comparison to a remainder of the first silicon dioxide on the vertical edge surfaces;

forming a silicon nitride layer on the first silicon dioxide adjacent the edge surfaces; and

forming a second silicon dioxide on the silicon nitride.

4. (Previously Presented) The method of claim 1, wherein disposing comprises forming respective polysilicon gates as the control gates.

5. (Previously Presented) The method of claim 1, wherein disposing comprises:
forming a first gate dielectric on an edge surface;
forming a charge trapping insulator on the first gate dielectric;
forming a second gate dielectric on the charge trapping insulator; and
forming a control gate on the second gate dielectric;
wherein the first gate dielectric, the charge trapping insulator and the second gate dielectric form a gate insulator.

6. (Previously Presented) The method of claim 1, wherein disposing comprises disposing structures each configured to store more than one bit per memory cell.

7-8. (Canceled)

9. (Original) The method of claim 1, wherein the semiconductor substrate comprises silicon.

10. (Canceled)

11. (currently amended) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:
doping a first region of a semiconductor substrate;
incising the substrate to provide an array of ~~substantially vertical~~ non-horizontal edge surfaces, pairs of the edge surfaces facing one another;
doping second regions of the substrate between the pairs of edge surfaces;
disposing ~~non-horizontal~~ structures, providing an electronic memory function, on the non-horizontal ~~on the substantially vertical~~ edge surfaces and second regions, wherein the ~~non-horizontal~~ structures each comprise an insulator structure having ~~first~~ non-horizontal portions, comprising a first oxide, formed on a pair of non-horizontal edge surfaces and a horizontal ~~second~~ portion formed on [[a]] the second region between the pair of non-horizontal edge surfaces, and a control gate coupled to the non-horizontal and horizontal ~~first and second~~ portions of the insulator structure, wherein the first oxide of each non-horizontal structure comprises a thicker portion only adjacent to the first region; and

establishing electrical contacts includes establishing electrical contacts to the first and second regions and to the control gates of the non-horizontal structures.

12. (currently amended) The method of claim 11, wherein disposing the ~~non-horizontal~~ structures on the non-horizontal ~~substantially vertical~~ edge surfaces comprises:
forming ONO structures on at least some of the pairs of edge surfaces; and
creating respective control gates on the ONO structures;
wherein the first oxide is ~~ONO structures each contain an oxide layer~~ formed on a pair of edge surfaces and on the ~~a~~ second region between that pair of edge surfaces.

13. (Canceled)

14. (Previously Presented) The method of claim 11, wherein the structures providing the electronic memory function are configured to store more than one bit per memory cell.

15. (currently amended) The method of claim 11, wherein disposing the ~~non-horizontal~~ structures comprises:
forming a first gate dielectric on a pair of the edge surfaces and a second region of the substrate between the pair of edge surfaces;
forming a charge trapping insulator on portions of the first gate dielectric adjacent the edge surfaces;
forming a second gate dielectric on the charge trapping insulator and a remaining portion of the first gate dielectric adjacent the second region; and
forming a control gate on the second gate dielectric
wherein the first gate dielectric, the charge trapping insulator and the second gate dielectric form the insulator structure.

16. (Canceled)

17. (Previously Presented) The method of claim 11, wherein disposing comprises forming respective polysilicon gates as the control gates.

18. (Canceled)

19. (Previously Presented) The method of claim 11, wherein disposing comprises disposing a structure that is configured to provide an electronic memory function by storing holes.

20. (currently amended) The method of claim 11, wherein disposing the ~~non-horizontal~~ structures comprises disposing substantially vertical structures.

21. (currently amended) A method for making an array of memory cells configured to store at least one bit per one F^2 comprising:

disposing non-horizontal structures providing an electronic memory function in trenches of a semiconductor substrate, wherein the structures providing the electronic memory function are configured to store more than one bit per gate and are composed of an oxide-nitride-oxide (ONO) gate dielectric formed under a control gate only along each sidewall of the trenches, wherein first oxide layers of the ONO gate dielectrics are formed on sidewalls and bottoms of the trenches such that only a portion of the first oxide layers along each sidewall is thicker than a remaining portion of the first oxide layer along each sidewall, and wherein the control gates are formed on second oxide layers of the ONO gate dielectrics; and

establishing electrical contacts to memory cells including the non-horizontal structures.

22. (Original) The method of claim 21, wherein disposing non-horizontal structures comprises disposing substantially vertical structures.

23. – 112. (Canceled)